FIG. 1

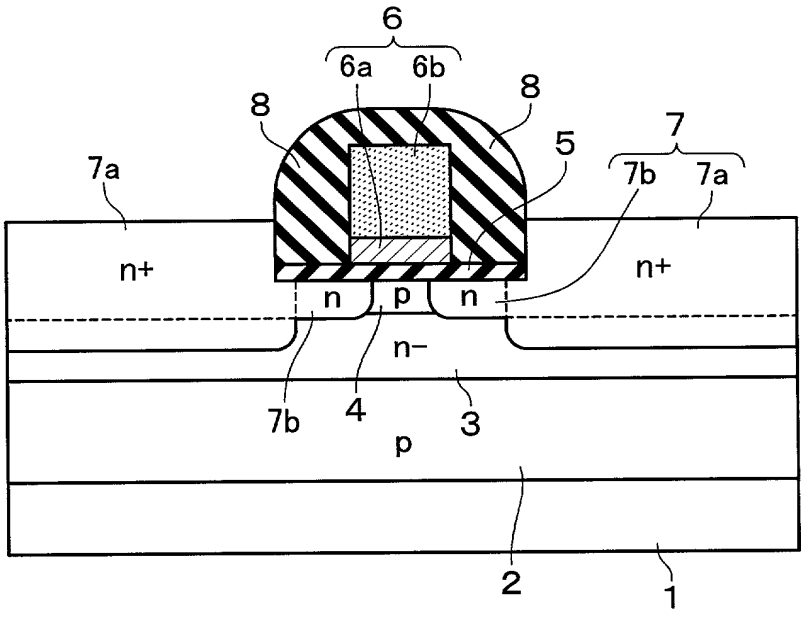

6
6a
6b
8
8
7
5
7a
7b
7a
n+
n+
n
p
n
n−
7b
4
3
p
2
1

FIG. 2

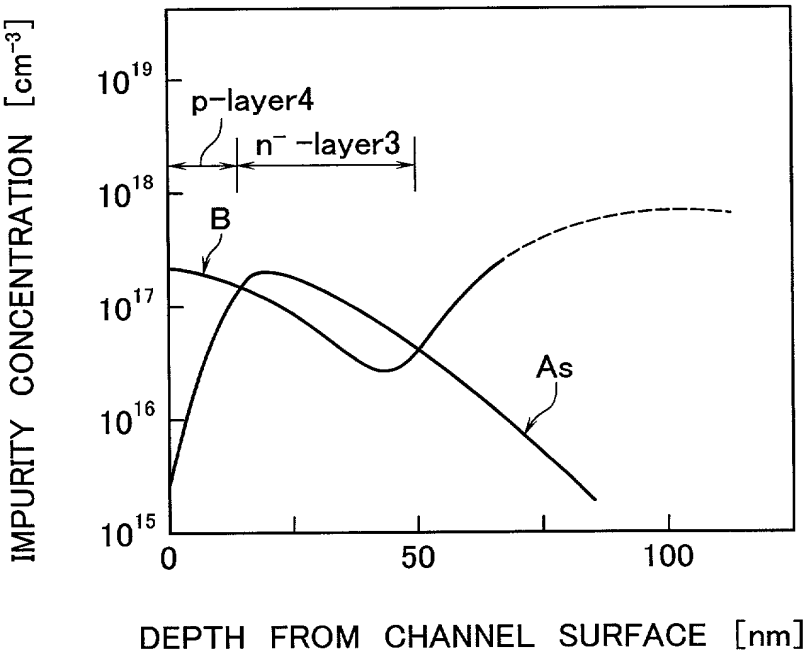

IMPURITY CONCENTRATION [cm⁻³]
10¹⁹
10¹⁸
10¹⁷
10¹⁶
10¹⁵
p−layer4
n⁻ −layer3
B
As
0
50
100
DEPTH FROM CHANNEL SURFACE [nm]

FIG. 3

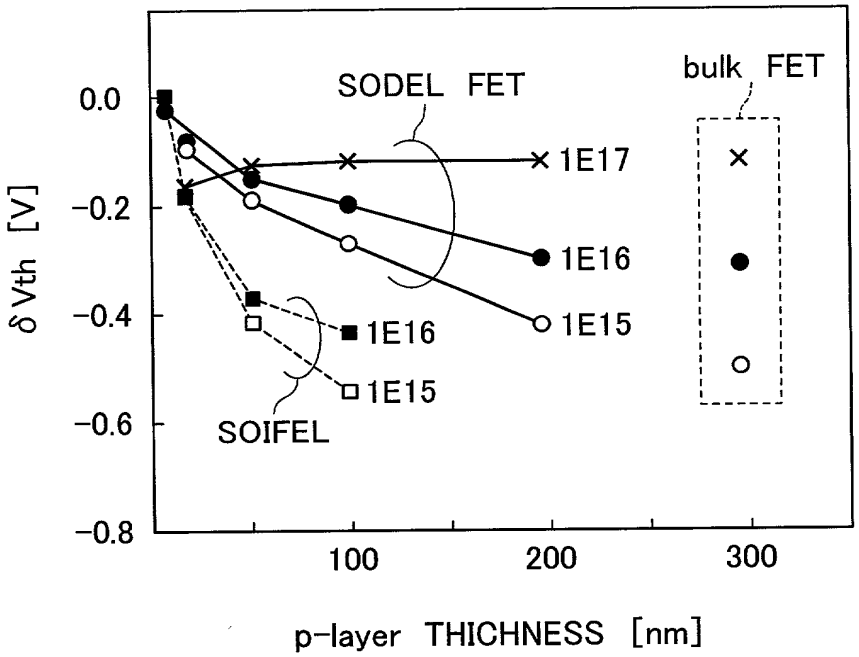

SODEL FET
bulk FET
1E17
1E16
1E15
1E16
1E15
SOIFEL
0.0
−0.2
−0.4
−0.6
−0.8
δ Vth [V]
100
200
300
p-layer THICHNESS [nm]

FIG. 4

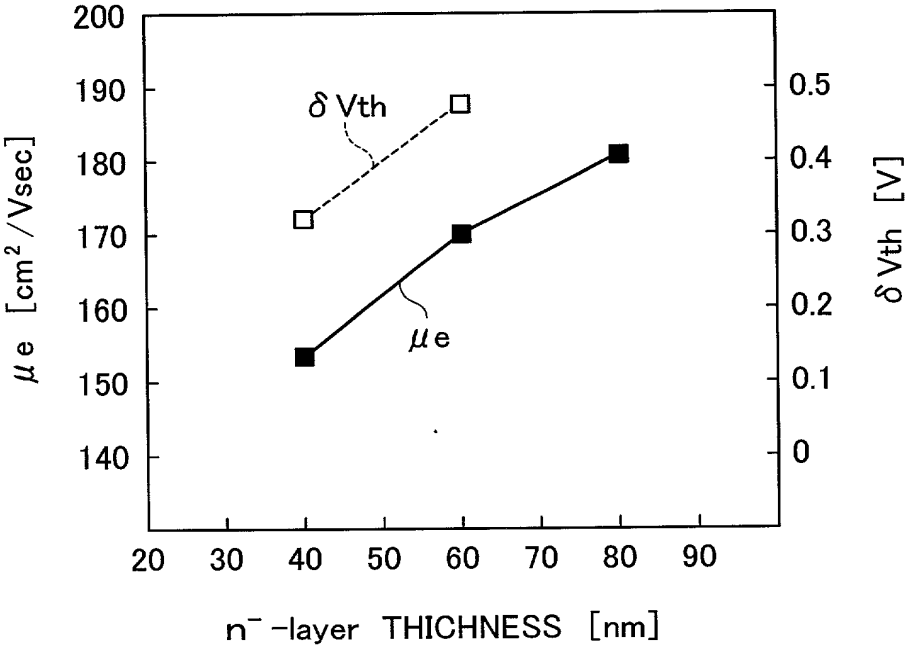

δ Vth
μe
200
190
180
170
160
150
140
μe [cm²/Vsec]
0.5
0.4
0.3
0.2
0.1
0
δ Vth [V]
20
30
40
50
60
70
80
90
n⁻-layer THICHNESS [nm]

FIG. 5A

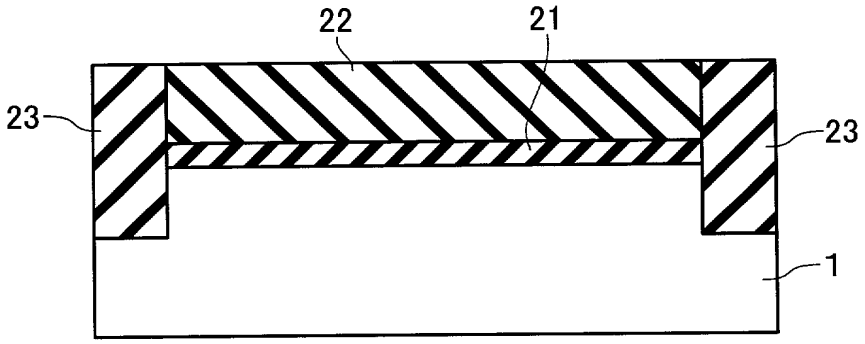


FIG. 5B

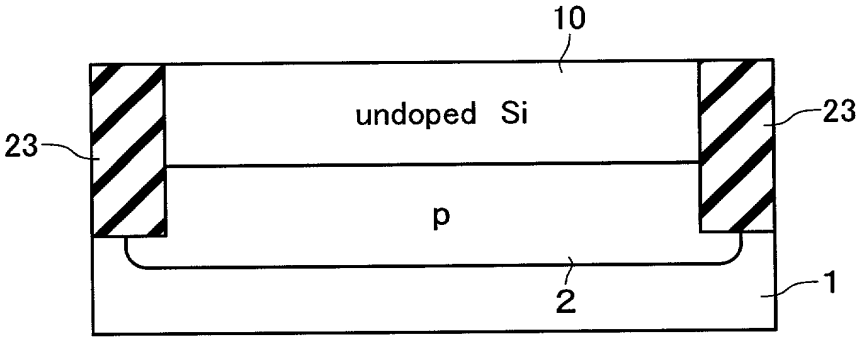


FIG. 5C

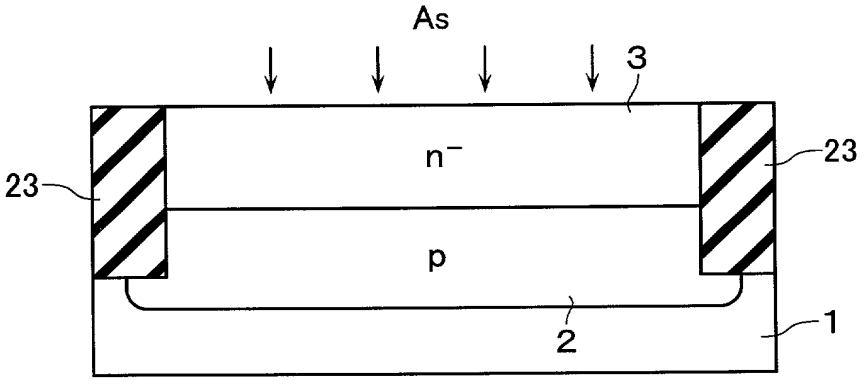


FIG. 5D

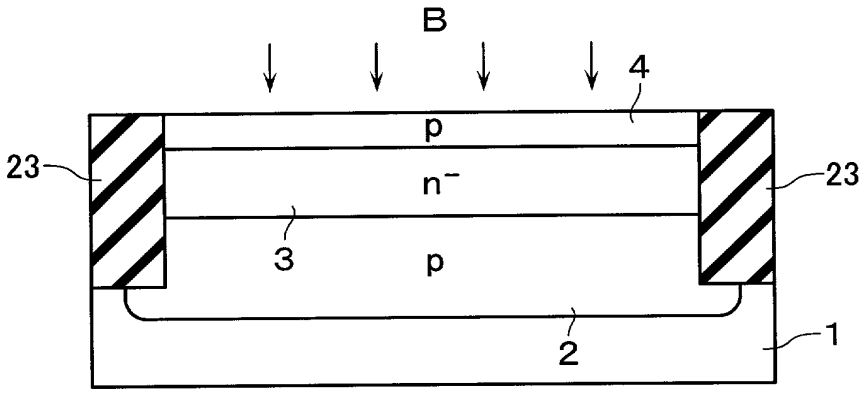


FIG. 6A

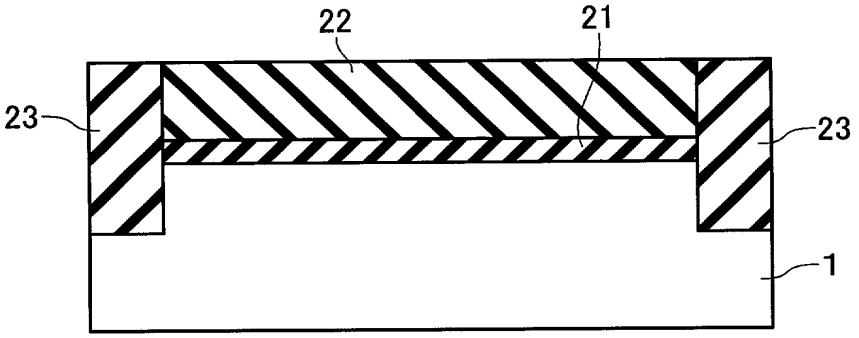


FIG. 6B

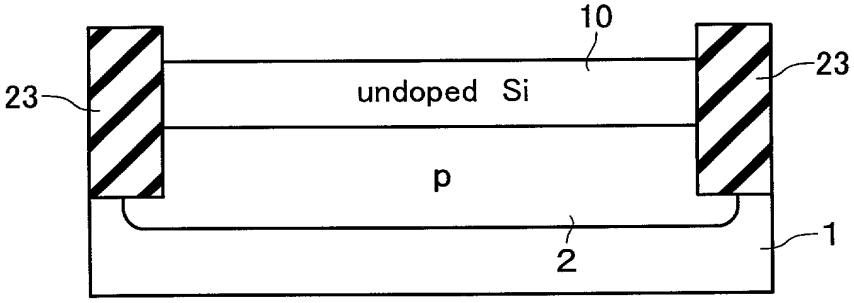


FIG. 6C

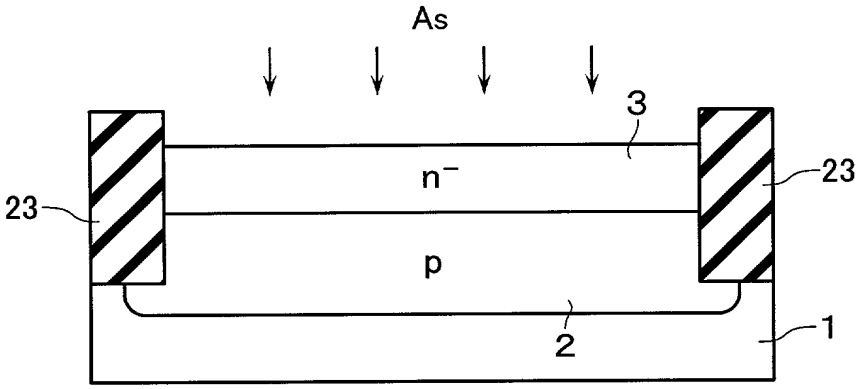


FIG. 6D

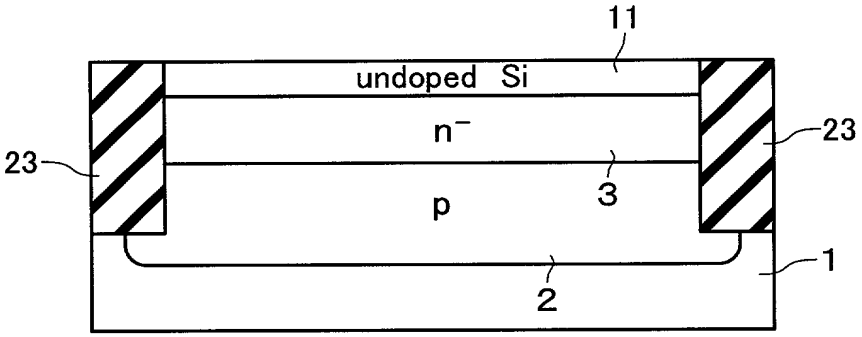


FIG. 6E

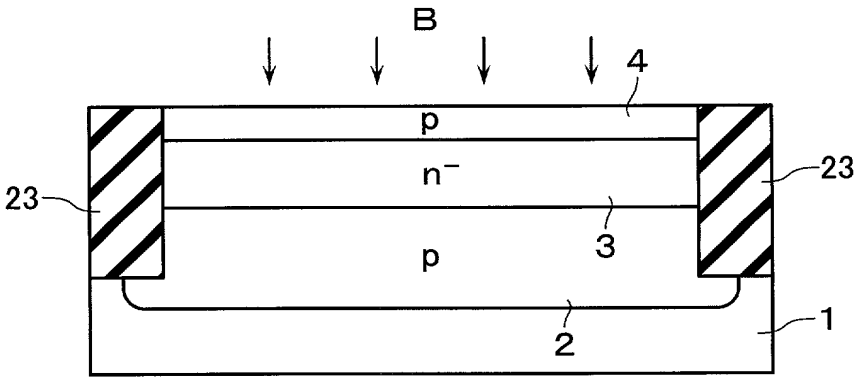


FIG. 7

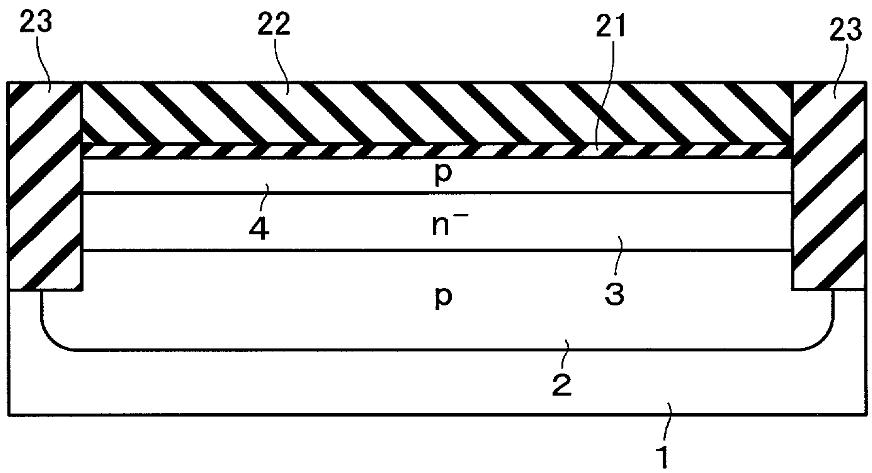


FIG. 8

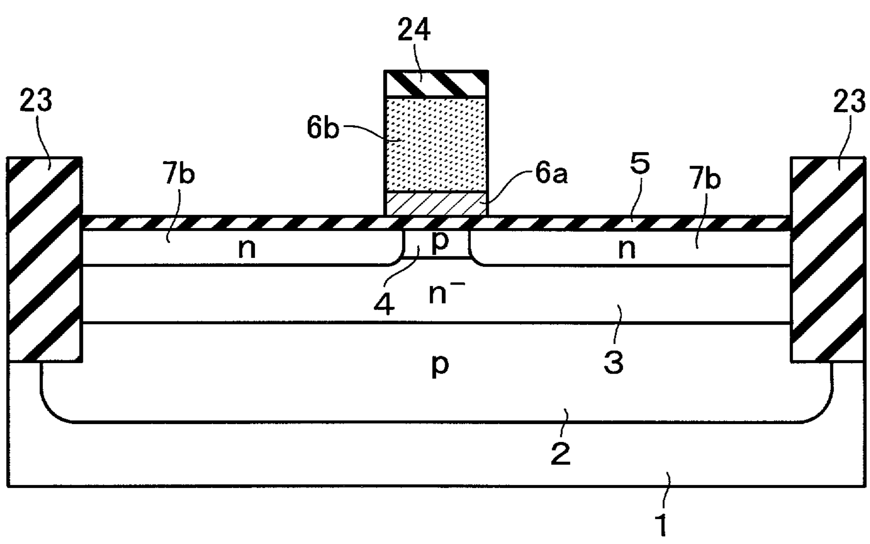


FIG. 9

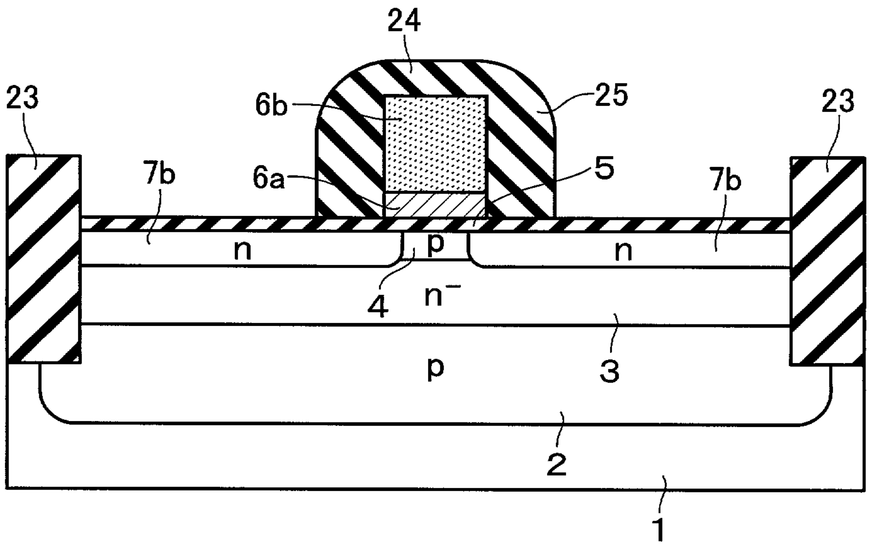

24
23
6b
25
23
7b
6a
5
7b
n
p
n
4
n⁻
p
3
2
1

FIG. 10

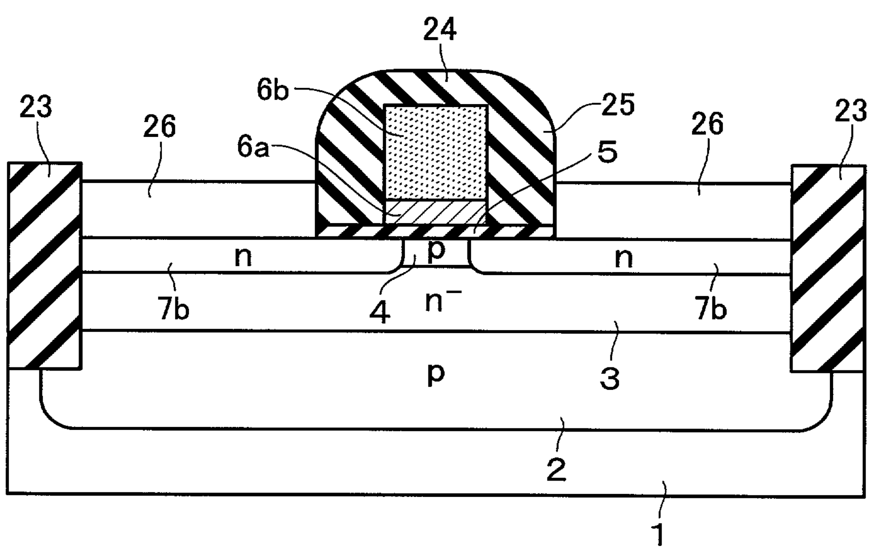

24
6b
25
23
26
26
23
6a
5
n
p
n
7b
4
n⁻
7b
p
3
2
1

FIG. 11

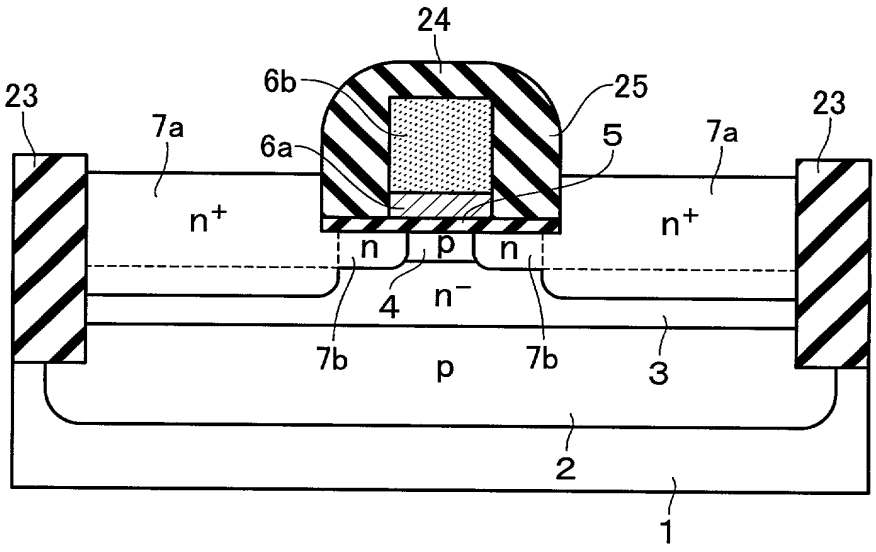

24
6b
25
23
7a
6a
5
7a
23
n+
n+
n
p
n
4
n−
7b
7b
p
3
2
1

FIG. 12

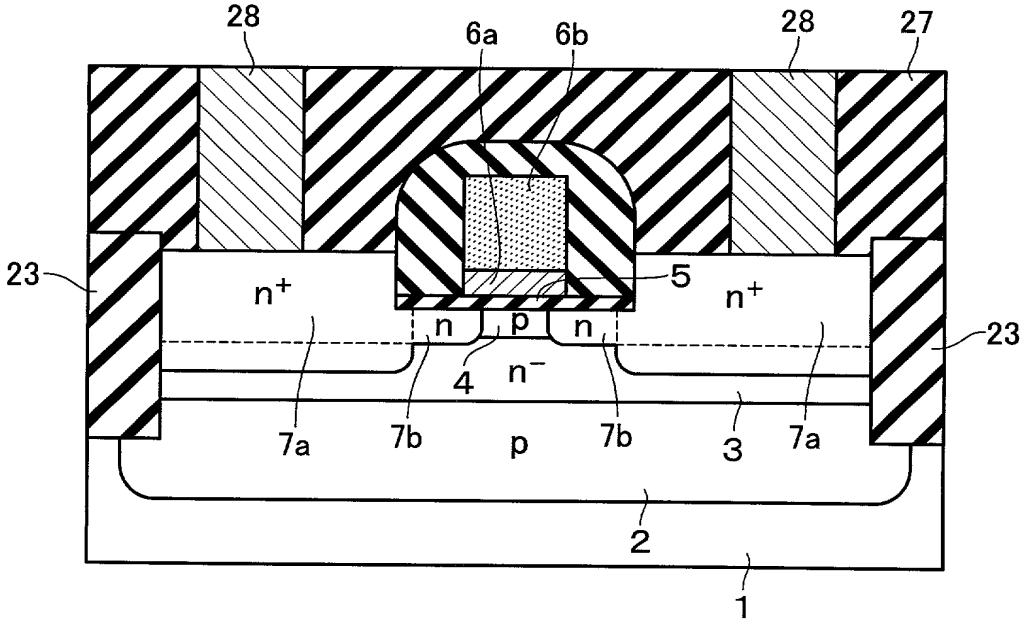

28
6a
6b
28
27
23
n+
5
n+
23
n
p
n
4
n−
7a
7b
7b
3
7a
p
2
1

FIG. 13

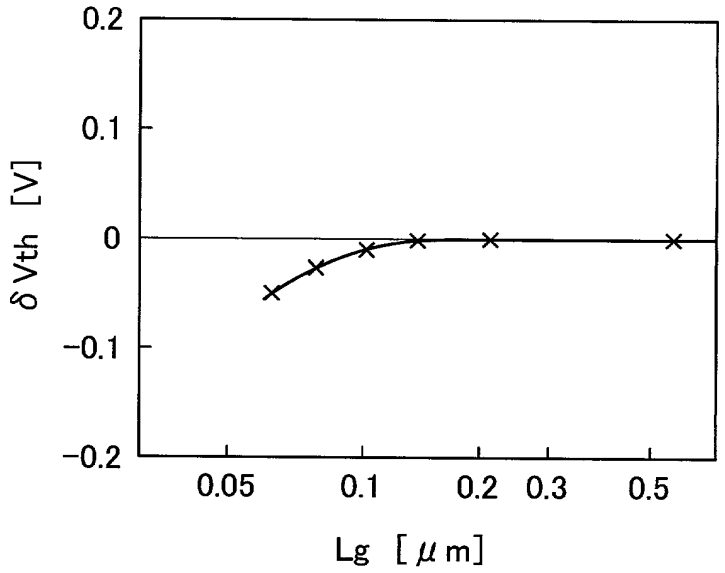


FIG. 14

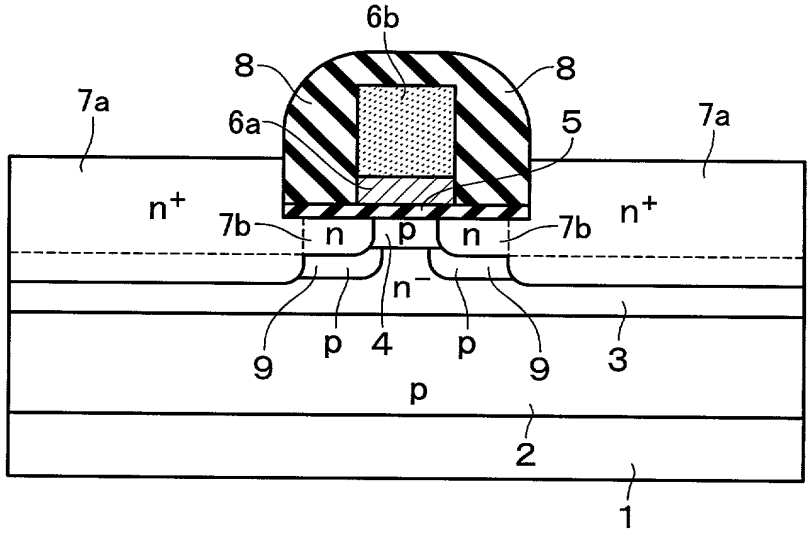


FIG. 15

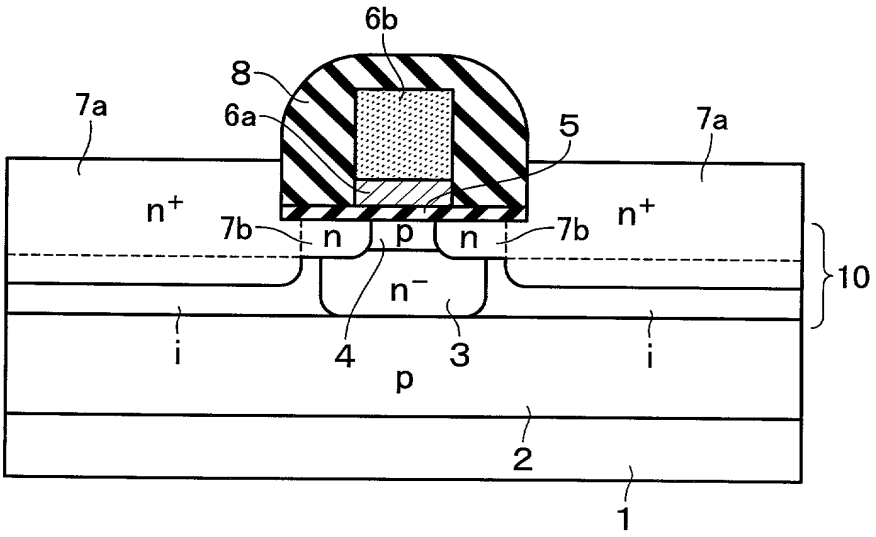


FIG. 16

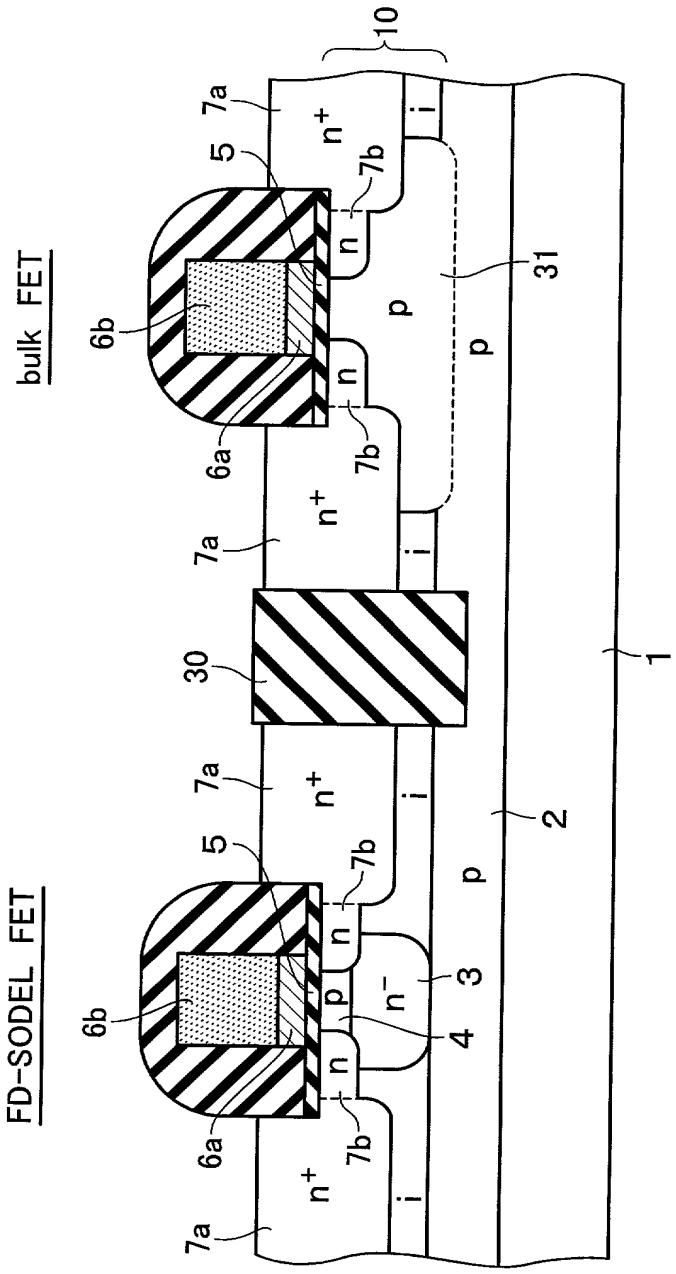


FIG. 17

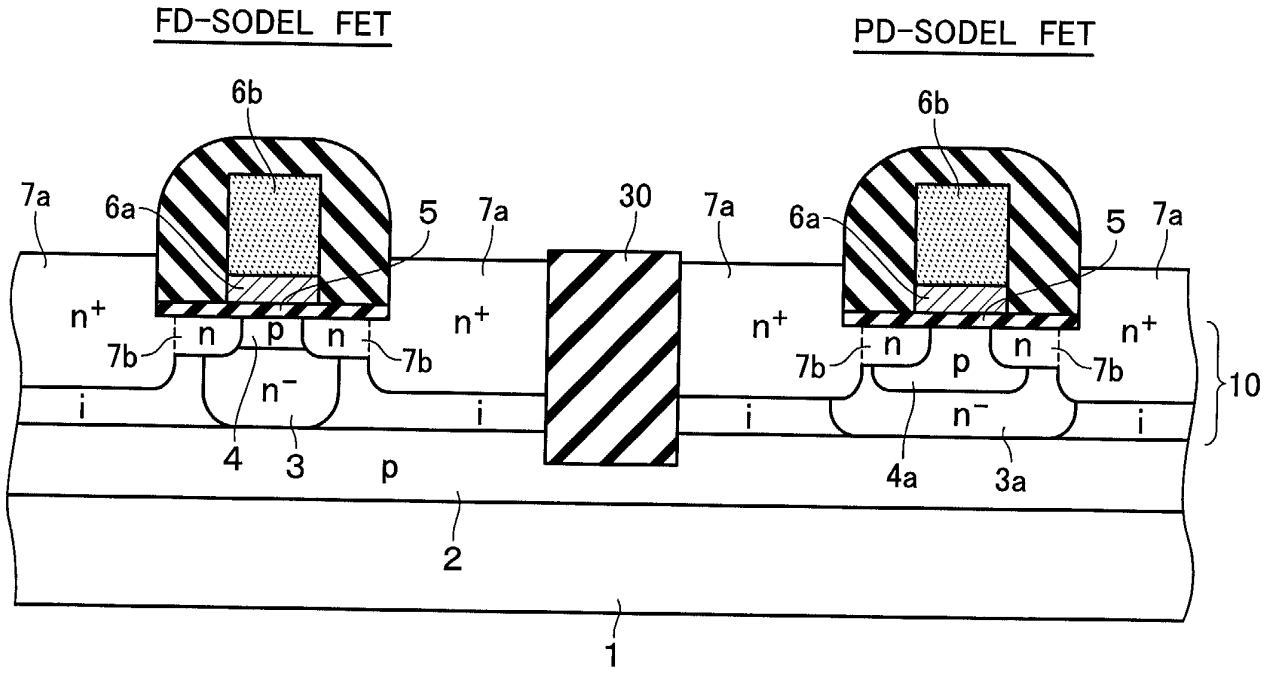


FIG. 18

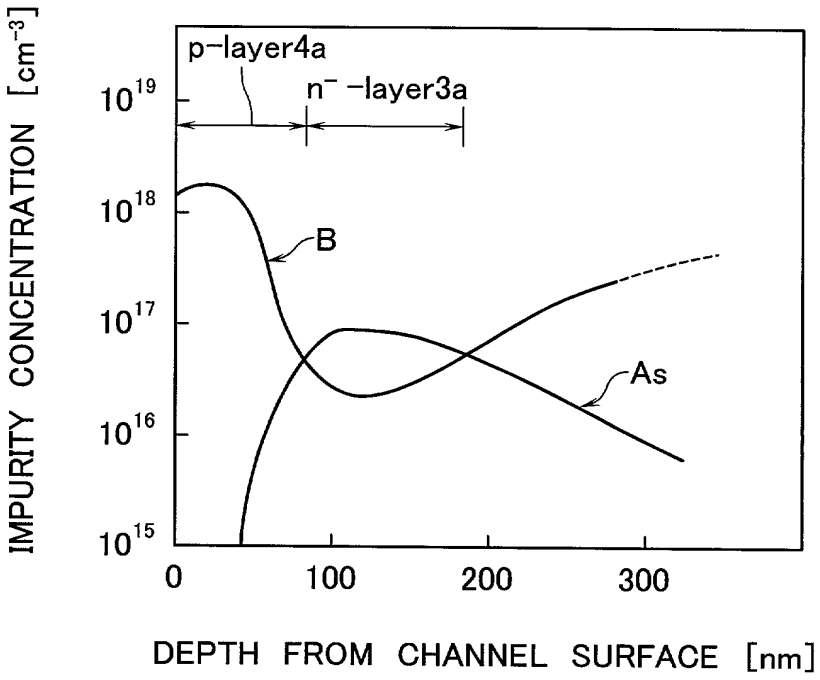

p-layer4a
n⁻ -layer3a
B
As
IMPURITY CONCENTRATION [cm⁻³]
10¹⁹
10¹⁸
10¹⁷
10¹⁶
10¹⁵
0
100
200
300
DEPTH FROM CHANNEL SURFACE [nm]

FIG. 19

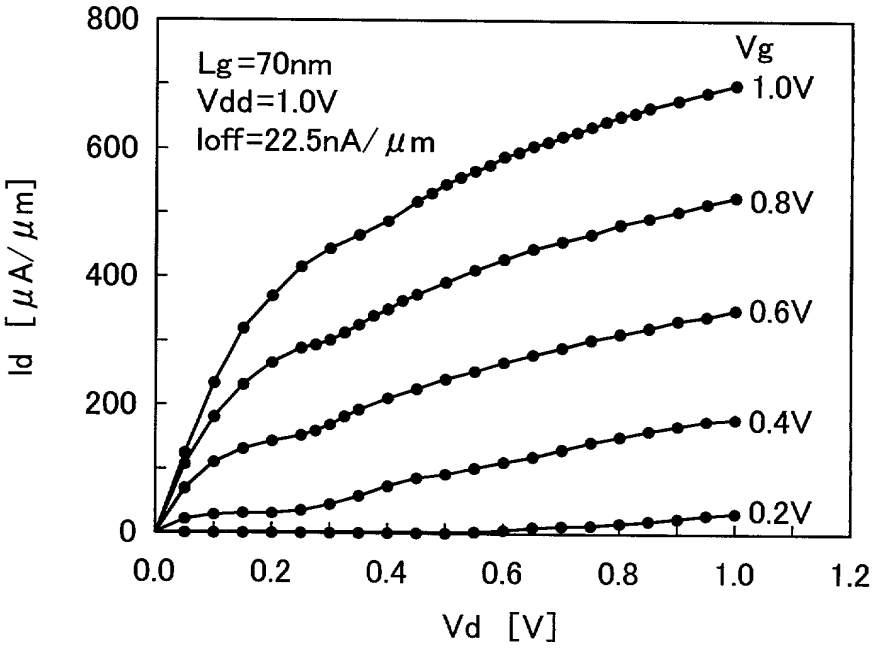

Lg=70nm
Vdd=1.0V
Ioff=22.5nA/μm
Vg
1.0V
0.8V
0.6V
0.4V
0.2V
Id [μA/μm]
800
600
400
200
0
0.0
0.2
0.4
0.6
0.8
1.0
1.2
Vd [V]

FIG. 20

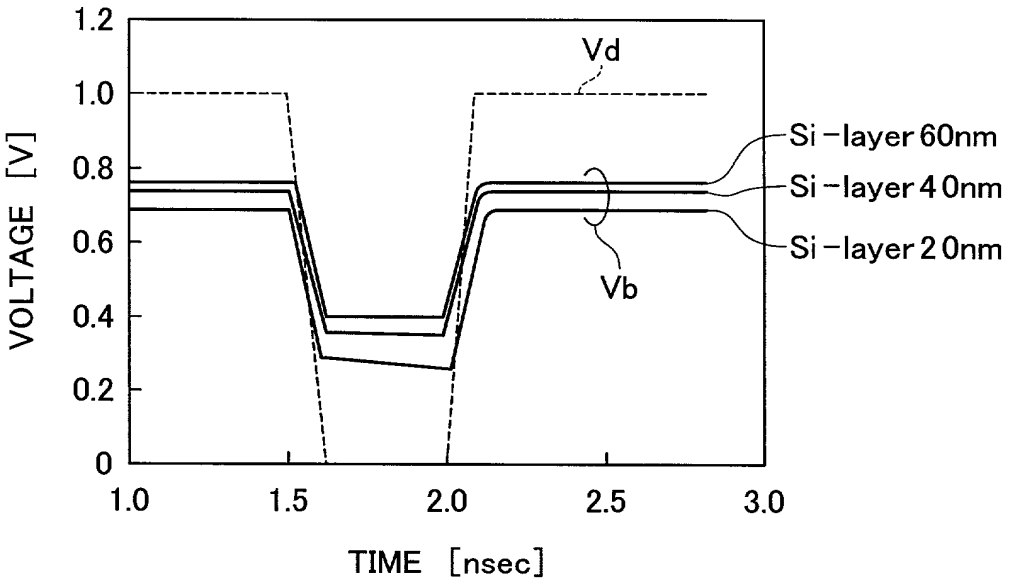

1.2
1.0
0.8
0.6
0.4
0.2
0
VOLTAGE [V]
1.0
1.5
2.0
2.5
3.0
TIME [nsec]
Vd
Vb
Si-layer 60nm
Si-layer 40nm
Si-layer 20nm

FIG. 22

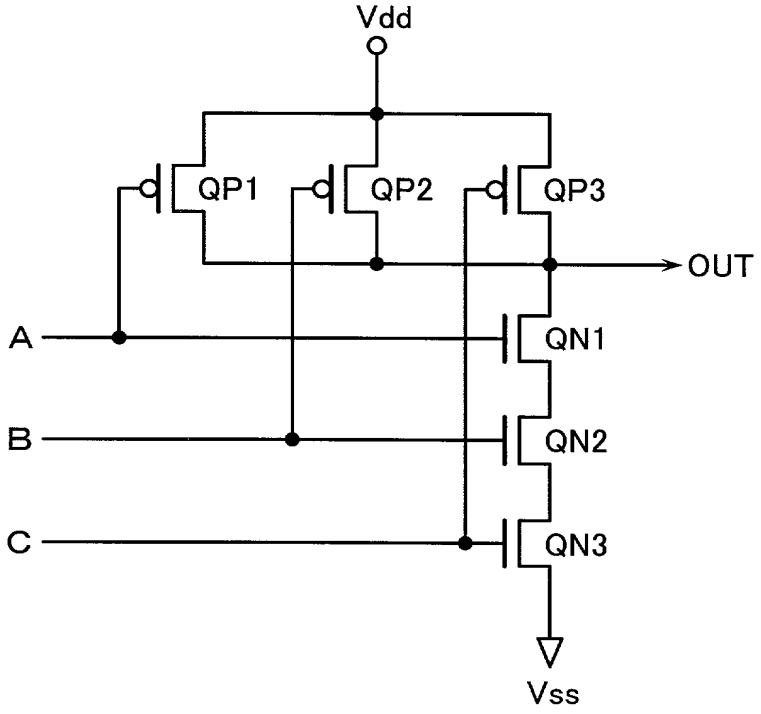

Vdd
QP1
QP2
QP3
OUT
A
B
C
QN1
QN2
QN3
Vss

FIG. 21

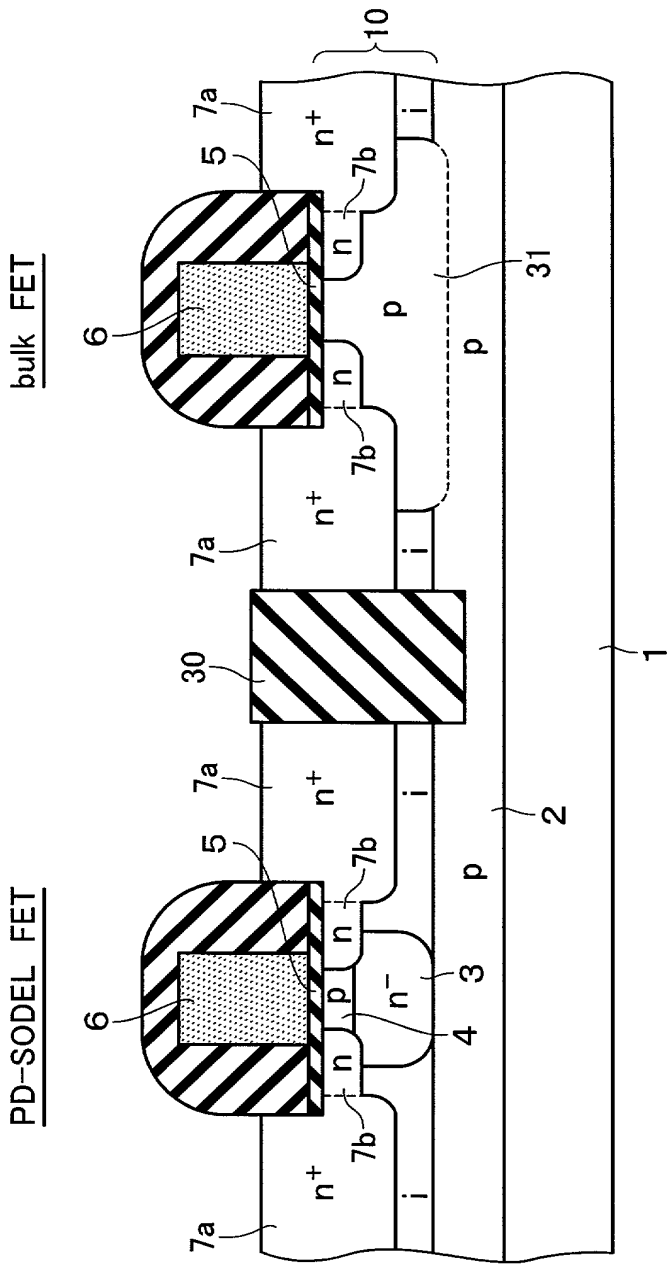


FIG. 23

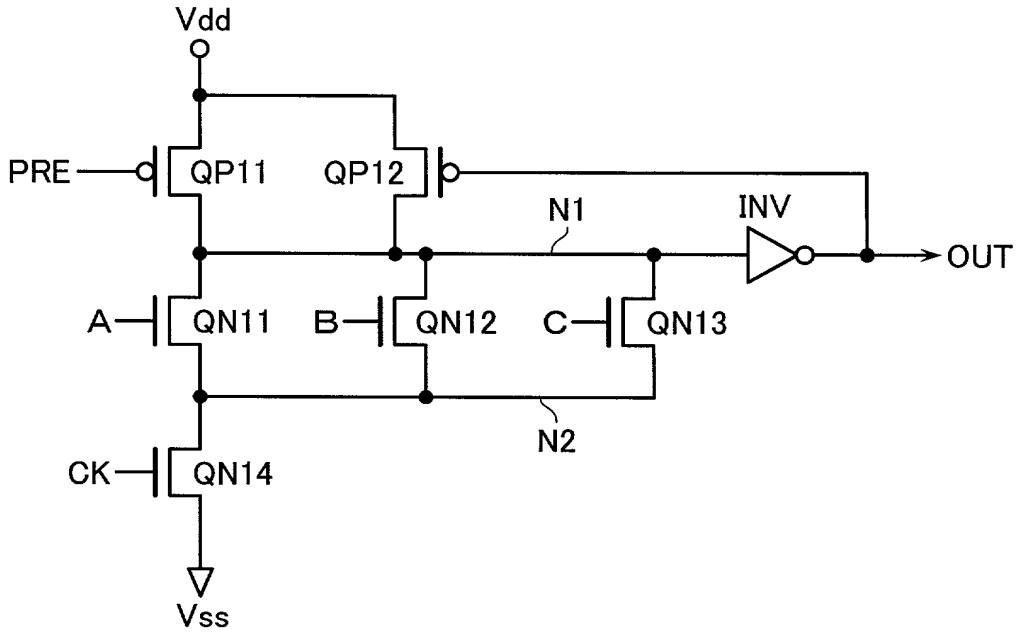

Vdd
PRE
QP11
QP12
N1
INV
OUT
A
QN11
B
QN12
C
QN13
N2
CK
QN14
Vss

FIG. 24

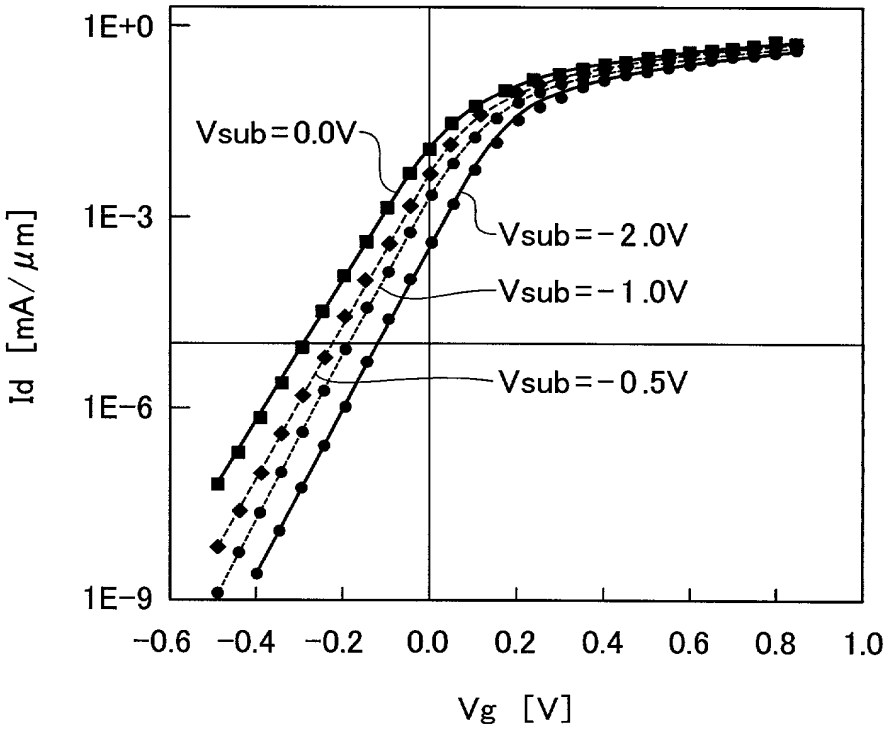
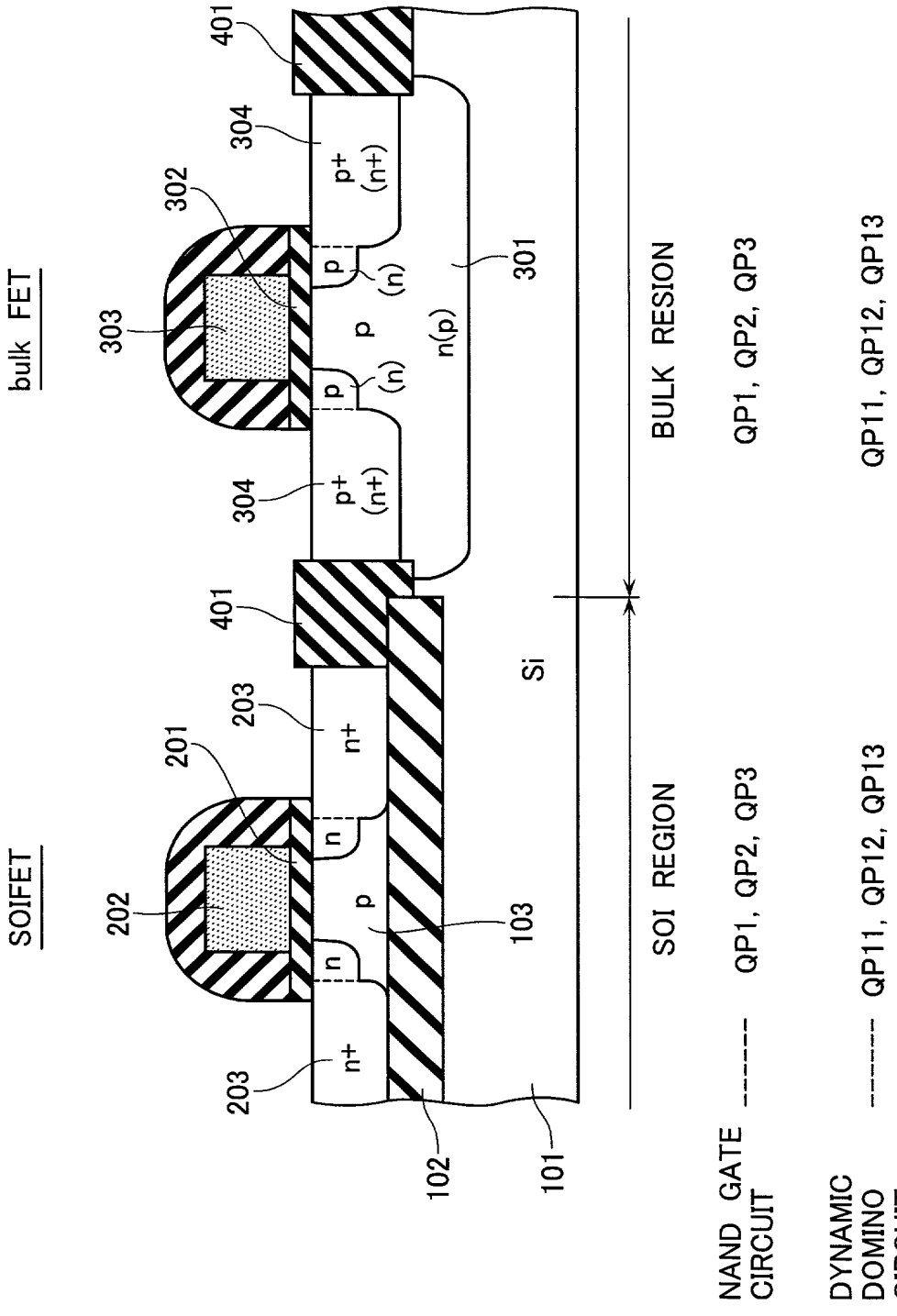

1E+0
1E−3
1E−6
1E−9
Id [mA/μm]
Vsub=0.0V
Vsub=−2.0V
Vsub=−1.0V
Vsub=−0.5V
−0.6
−0.4
−0.2
0.0
0.2
0.4
0.6
0.8
1.0
Vg [V]

FIG. 25


SOIFET
bulk FET
202
201
203
n+
n
p
n
n+
203
102
103
101
Si
401
304
p+
(n+)
302
303
p
(n)
p
(n)
n(p)
301
304
p+
(n+)
401
SOI REGION
BULK RESION
NAND GATE CIRCUIT
QP1, QP2, QP3
QP1, QP2, QP3
DYNAMIC DOMINO CIRCUIT
QP11, QP12, QP13
QP11, QP12, QP13